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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ARENA, ANDREW OWENS	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,235	SHIMIZU, KAZUHIRO	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/24/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicants regard as their invention. Evidence that claim 5 fails to correspond in scope with that which applicants regard as the invention can be found in the originally filed drawings and specification.

Applicant has defined an in-line portion (Fig 16: 80a; pg 25 ln 8), a first trench isolation structure (8a; pg 10 ln 25) having an in-line portion (80a), and a second trench isolation structure (8b; pg 11 ln 10). Clearly, the second trench isolation structure exists entirely within the first impurity region (3). It seems the in-line portion is perpendicular to the second trench isolation structure. The recitation "second trench isolation structure...comprise an in-line portion which extends from said first impurity region towards said second impurity region" (ln 2-3) is unclear, rendering the claim indefinite.

For art-based rejection purposes, the claim will be given the most reasonable interpretation consistent with applicant's drawings and specification.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action (non-final rejection dated 11/15/2005).

Claims 1, 2, 6, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terashima (US 5,894,156) in view of Nagatani (US 6,376,891).

Regarding claim 1, Terashima discloses a semiconductor device (Fig 12; col 1) comprising:

a semiconductor substrate (1; ln 22) of a first conductivity type (p);

a semiconductor layer (2; ln 22) of a second conductivity type (n) provided on said semiconductor substrate;

a first impurity region (leftmost 3; ln 22) of said first conductivity type (p) provided in said semiconductor layer, extending from an upper surface of said semiconductor layer to reach an interface with said semiconductor substrate, said first impurity region defining a RESURF isolation region (everything right of leftmost 3);

a first trench isolation structure (trench containing rightmost 3) provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region (via substrate 1), extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said first trench isolation structure and said first impurity region together defining a first trench isolation region (between 3s) in said RESURF isolation region;

a semiconductor element (6; ln 24) provided in said semiconductor layer defined in said RESURF isolation region excluding said first trench isolation region; and

a first MOS transistor (nch RESURF MOSFET; ln 19), comprising

a second impurity region (5 right of 9) of said second conductivity type (n) provided in said upper surface of said semiconductor layer defined in said first trench isolation region, said second impurity region being connected to a drain electrode (8) of said first MOS transistor,

a third impurity region (6) of said first conductivity type (p) provided in said upper surface of said semiconductor layer defined between said first and second impurity regions, and

a first source region (leftmost 5) of said second conductivity type (n) provided in an upper surface of said third impurity region,

wherein said semiconductor device further comprises a buried impurity region (4) of said second conductivity type (n) provided below said second impurity region and at said interface between said semiconductor layer and said semiconductor substrate, said buried impurity region being higher in impurity concentration than said semiconductor layer.

Further regarding claim 1, Terashima differs from the claimed invention only in not disclosing said buried impurity region provided "directly below" said second impurity region. Nagatani discloses (Fig 1) a buried impurity region (2; col 9 ln 33) provided directly below the second diffusion region. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Terashima such that a buried impurity region is provided directly below said second impurity region, as taught by Nagatani; at least to accommodate a low breakdown voltage MOSFET (Nagatani: col 10 ln 41-49, col 2 ln 21-27, col 2 ln 42-46, col 3 ln 5-7).

Regarding claim 2, Terashima discloses (Fig 12) a second trench isolation structure (trench containing leftmost 3) separated by a certain distance from said first trench isolation structure, said second trench isolation structure being provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region (trench sidewalls connected to impurity region contained therein), extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said second trench isolation structure, said first impurity region, and said first trench isolation structure together defining said first trench isolation region (between 3s) in said RESURF isolation region.

Regarding claim 6, Terashima discloses (Fig 12) wherein said first trench isolation structure (trench containing rightmost 3) reaches said semiconductor substrate (1), and wherein an end portion of said first trench isolation structure reaches a depth shallower than the greatest possible depth (same depth as 4) of said buried impurity region.

Regarding claim 9, Terashima discloses (Fig 7) a second isolation structure (separating MOSFET from island region) and a second MOS transistor, further disclosing (Fig 12):

said second trench isolation structure (trench containing rightmost 3) provided in said semiconductor layer defined in said RESURF isolation region to be connected to said first impurity region (via substrate 1), extending from said upper surface of said semiconductor layer to reach at least the vicinity of said interface with said semiconductor substrate, said second trench isolation structure and said first impurity

region together defining a second trench isolation region (between 3s) in said RESURF isolation region, and

a second MOS transistor (nch RESURF MOSFET; ln 19), comprising

a fourth impurity region (5 right of 9) of said second conductivity type (n) provided in said upper surface of said semiconductor layer defined in said second trench isolation region, said fourth impurity region being connected to a drain electrode (8) of said first MOS transistor,

a fifth impurity region (6) of said first conductivity type (p) provided in said upper surface of said semiconductor layer defined between said first and fourth impurity regions, and

a second source region (leftmost 5) of said second conductivity type (n) provided in an upper surface of said fifth impurity region.

Regarding claim 10, Terashima discloses (Fig 12; col 1) an interconnect line (8; ln 25) provided over said first trench isolation structure to be electrically connected to said drain electrode (portion of 8 contacting 5 is drain electrode), and

a field plate (11; ln 49) held between said first trench isolation structure and said interconnect line,

wherein said field plate is a floating electrode (ln 51).

Claims 3-5, 7, 8, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terashima in view of Nagatani as applied to claims 1, 2, and above, and further in view of Leonardi (US 6,798,037).

Regarding claim 3, Terashima discloses (Fig 1) said first trench isolation structure comprises an in-line portion (top and bottom horizontal trenches separating MOSFET from Island Region) which extends from said first impurity region towards said second impurity region, but differs from the claimed invention only in not disclosing "a plurality of spaced-apart conductive films" and "a plurality of first insulating films".

Leonardi discloses (Fig 4) an isolation structure (col 4 ln 17-20) including a plurality of spaced-apart conductive films (5*; col 4 ln 32-33) in a semiconductor layer, and a plurality of first insulating films (4*; col 4 ln 30) for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Terashima such that said in-line portion includes:

a plurality of spaced-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of first insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer,

in view of the teaching of Leonardi; at least to prevent parasitic effects of junction isolation (Leonardi: col 4 ln 50-53).

Regarding claim 4, Terashima as modified by Leonardi discloses openings (Leonardi - Fig 5C) between adjacent ones of said plurality of conductive films are filed with said plurality of first insulating films (Leonardi - Fig 5E: 4*).

Regarding claim 5, Terashima discloses (Fig 12) said second trench isolation structure comprises an in-line portion (the trench containing leftmost 3) which extends within said first impurity region and said first trench isolation structure comprises an in-line portion (top and bottom horizontal trenches separating MOSFET from Island Region) which extends from said first impurity region towards said second impurity region, but differs from the claimed invention only in not disclosing "a plurality of spaced-apart conductive films" and "a plurality of insulating films".

Leonardi discloses (Fig 4) an isolation structure (col 4 ln 17-20) including a plurality of spaced-apart conductive films (5*; col 4 ln 32-33) in a semiconductor layer, and a plurality of insulating films (4*; col 4 ln 30) for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Terashima such that said in-line portion (of said first trench isolation structure) includes:

a plurality of spaced-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer,

in view of the teaching of Leonardi; at least to prevent parasitic effects of junction isolation (Leonardi: col 4 ln 50-53).

Regarding claim 7, Terashima discloses said first trench isolation structure comprises an in-line portion (top and bottom horizontal trenches separating MOSFET from Island Region) which extends from said first impurity region towards said second impurity region, wherein said semiconductor device further comprises a fourth impurity region (rightmost 3) provided in said upper surface of said semiconductor layer defined in said RESURF region, but differs from the claimed invention only in not disclosing "a plurality of spaced-apart conductive films" and "a plurality of first insulating films".

Leonardi discloses (Fig 4) an isolation structure (col 4 ln 17-20) including a plurality of spaced-apart conductive films (5*; col 4 ln 32-33) in a semiconductor layer, and a plurality of insulating films (4*; col 4 ln 30) for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer. Leonardi further teaches that junction isolation is known (col 1 ln18-20).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Terashima such that said in-line portion (of said first trench isolation structure) includes:

a plurality of spaced-apart conductive films provided in said semiconductor layer defined in said RESURF isolation region, aligning in the extending direction of said in-line portion, and

a plurality of insulating films for covering respective ones of said plurality of conductive films, at surfaces buried in said semiconductor layer, and

said fourth impurity region surrounds each one of said plurality of insulating films while filling openings between adjacent ones of said plurality of insulting films,

in view of the teaching of Leonardi; at least to prevent parasitic effects of junction isolation (Leonardi: col 4 ln 50-53).

Regarding claim 8, Terashima as modified by Leonardi discloses applicant's claimed structure, and is therefore inherently capable of performing applicant's claimed function:

said fourth impurity region is depleted in its entirety when a PN junction between said fourth impurity region and said semiconductor layer is subjected to application of a reverse voltage.

Regarding claim 11, Terashima as modified by Nagatani and Leonardi discloses (Terashima: Fig 12)

a second insulating film (7) provided on said semiconductor layer (2) defined between said first impurity region (leftmost 3) and said buried impurity region, and

a plurality of field plates (11; ln 49-51) provided on said second insulating film,

wherein said plurality of conductive films are exposed from said upper surface of said semiconductor layer (Leonardi – Fig 4: 5*; col 4 ln 38-40),

wherein said plurality of field plates are respectively connected (indirectly) to said plurality of conductive films (all features formed in a common substrate are connected).

Response to Arguments

Applicant's arguments filed 02/09/2006 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Wada (US 6,274,919) discloses (Fig 1A; col 4) a trench isolation structure (11; ln 23) comprising conductive films (6; ln 32) and insulating films (5; ln 33) for covering respective ones of conductive films.

Stengl (US 5,113,237) discloses (Fig 1; col 3) an isolation scheme wherein field plates (12-14; ln 43) are electrically connected to underlying isolation regions (ln 61), and teaches the advantage of doing so (col 1 ln 32-34, 40-43).

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is (571) 272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOA
27 April 2006

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